



# AlN Laser Diode Carriers

Thin film metallised Aluminium Nitride (AlN) submounts/carriers for mounting of laser diodes and associated components and devices for optical sub-assemblies.

## Ceramic material

The ceramic substrate material is Aluminium Nitride (AlN). Standard grade is 170W/m·K. 200W/m·K is also available. Typical properties are:

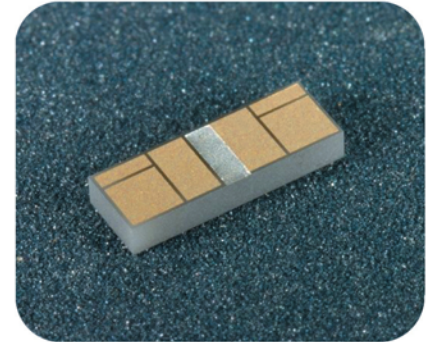
TC (W/m·K)	~170
CTE (ppm/°C)	~4.6
Dielectric constant	~8.8 @ 1MHz

### Thickness, flatness and surface finish

The AlN substrate material is available with as-fired, lapped or polished surface finishes. Standard substrate thicknesses are 0.63mm and 1.0mm with as-fired finish. Non-standard thickness material can also be fabricated. Substrates can be lapped and polished from 0.25mm thick up to 1.5mm thick.

The flatness and surface finish of the substrate material affects conductor definition and adhesion and also the quality of the laser die attachment. Typical substrate properties are:

Surface	Thickness	Flatness	Surface Finish	Notes
As-fired	±15%	50 µm/25 mm	~1.6 µm Ra	Lowest cost
Lapped	±0.02 mm	5 µm/25 mm	~1.0 µm Ra	Better thickness and flatness control but poor surface integrity
Near polish	"	"	~0.15 µm Ra	Best for conductor and AuSn adhesion
Polished	"	"	<0.05 µm Ra	Best for conductor definition and minimising epoxy bleedout



## Mechanical dimensions

Small mounts are commonly used for individual chip-on-carrier assemblies, and large substrates with complex patterning for optical sub-assemblies. General size limits are:

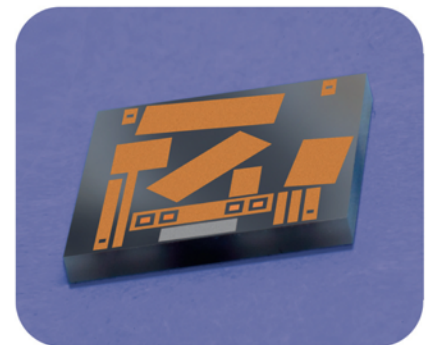
Min. length and width	0.5 mm x 0.5 mm
Max. length and width	75 mm x 75 mm

Parts can be machined using diamond saws for the highest edge quality and dimensional control. Laser profiling/scrubbing are used for complex shapes, holes, etc. Typical tolerances available:

Diamond sawing:	Typical	High spec.
Length and width	±0.05 mm	±0.02 mm
Edge chipping	<0.05 mm	<0.02 mm
Pattern to edge	±0.05 mm	±0.01 mm

Laser profiling:	Typical	High spec.
Holes	±0.05 mm	±0.025 mm
Pattern to edge/feature	±0.05 mm	±0.025 mm



## Metallisations

Various metallisation schemes can be applied to form conductors, integral resistors, solder barriers, solder dams etc. Typical schemes include:

Conductors	Notes
Ti/Pt/Au	Best overall conductor scheme but highest cost
TiW/Pd/Au (+ Au)	Pd barrier layer (plus electroplated Au) for standard low cost scheme
TiW/Au (+ Ni/Au)	Ni barrier layer for extra protection when soldering with Sn and Pb based solders
TiW/Au (+ Au)	For high temperature soldering. Suitable for Au bearing solders only

Resistors	Notes
Ta2N or NiCr	Typical sheet resistivity of 50 ohms per sq, with a standard tolerance of 20% or 0.2% if laser trimmed

Dielectrics	Notes
Polyimide	For conductor cross overs, solder dams and passivation protection

The Au and barrier layer thicknesses depend on the application. Generally for Au wire bonding 0.5µm minimum of Au is required. For Pt or Pd barrier layers a minimum of 0.2µm is usually specified.

## Plated thru-holes (substrate vias)

Front and back faces of the component can be electrically interconnected using pre-drilled metallised thru-holes. Typical hole diameter = substrate thickness.

## Wrap around metallisation

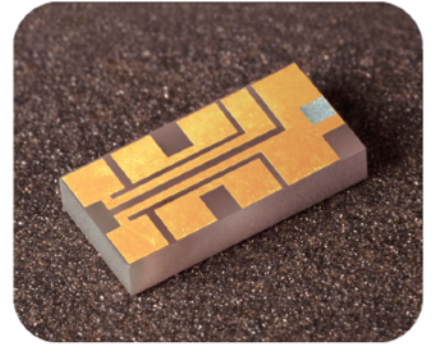
Plain submounts can also be fabricated with metallisation that wraps around one or multiple sides walls to connect the top and bottom faces. Wrap around connections can also be accomplished on patterned mounts, with due consideration to process limitations and cost.

## Patterning

Circuit features are realised using wet or dry film resists and chemical or plasma etching. Typical capabilities:

Minimum line width	25 $\mu\text{m}$
Minimum gap width	25 $\mu\text{m}$
Line width tolerance	$\pm 10 \mu\text{m}$
Line to feature (e.g. hole)	$\pm 50 \mu\text{m}$

Alignment guides/fiducials can be incorporated into the design for subsequent automated assembly.



## Pre-deposited AuSn

For laser mounting a thin layer of vacuum-deposited AuSn can be selectively applied over conductor areas. The standard alloy ratio is nominally 76Au/24Sn, normally at ~4-5 microns thick. On reflowing, the Au in the underlying conductor and on the underside of the laser chip, combine with the pre-deposited solder to form an alloy approximating to the eutectic ratio of 80Au/20Sn. The resulting alloy flows and wets very well to both the laser and the carrier, resulting in excellent low-void joints minimising thermal resistance and hotspots. The alloy ratio can also be tailored for specific applications. Typical AuSn features:

Min. length or width	100 $\mu\text{m}$
Thickness	3-5 - 5.5 $\mu\text{m}$
Alignment to conductors	$\pm 10 \mu\text{m}$

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Images are not to scale

LEW Techniques specialises in the manufacture of miniature components for the mounting of semiconductor devices. Our in-house capabilities include Thin Film, Thick Film and refractory metallising of ceramics and metals, electroplating, precision dicing, laser machining and marking, atmosphere/vacuum brazing and solder assembly.

To ensure end user compatibility, comprehensive in-house testing includes eutectic die bonding, Au wire bonding, shear strength, peel strength, coating thickness and surface finish measurement, heat testing and He leak detection.

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